

## High Speed-10 MBit/s Logic Gate Optocouplers

### 1.Description

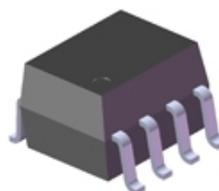
The SL0601 optocouplers consists of an 850nm AlGaAs LED, optically coupled to a very high speed integrated photo-detector logic gate that quickly outputs. This device is housed in an 8-pin standard package, conforming to the standard package outline.

### 2.Features

- Very high speed-10 MBit/s
- High isolation voltage between input and output ( $V_{iso}=3750V_{rms}$ )
- Range of working temperature:  $-40^{\circ}C \sim 85^{\circ}C$
- Logic Gate Output
- Storable output

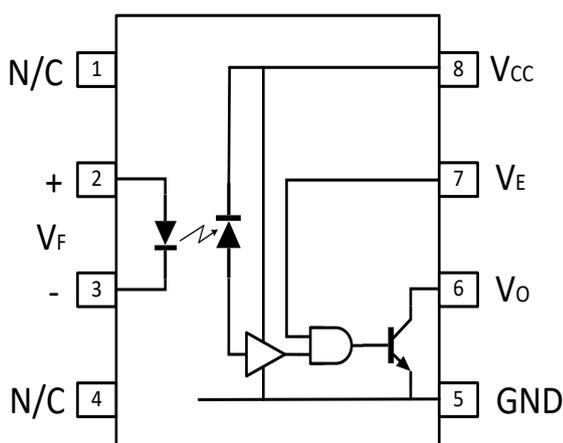
### 3.Applications

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line Receiver, Data Transmission
- Data Multiplexing
- Switching Power Supplies
- Pulse Transformer Replacement
- Computer-peripheral Interface



SOP-8

### 4.Structural schematics and packaging



TRUTH TABLE (Positive Logic)		
Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

## 5. Absolute Maximum Ratings (Unless otherwise specified, $T_A = 25$ )

Exceeding the absolute maximum ratings may damage the device. It is recommended that the device not operate beyond the specified operating conditions, as this may affect the device's functionality. Additionally, prolonged operation beyond the recommended operating conditions may impact the device's reliability.

Symbol	Parameter	Value	Units
$T_{STG}$	Storage temperature	-55 to +125	°C
$T_{OPR}$	Operating temperature	-40 to +85	°C
$T_{SOL}$	Soldering temperature	260 for 10 sec	°C
<b>EMITTER</b>			
$I_F$	Forward input current	50	mA
$V_E$	Enable input voltage. Not to exceed $V_{CC}$ by more than 500 mV	5.5	V
$V_R$	Reverse input voltage	5.0	V
$P_I$	Power dissipation	100	mW
<b>DETECTOR</b>			
$V_{CC}$ (1 minute max)	Supply voltage	7.0	V
$I_O$	Output current	50	mA
$V_O$	Output Voltage	7.0	V
$P_O$	Collector output power dissipation	85	mW

## 6. Recommended operating conditions

The recommended operating conditions table specifies the recommended operating conditions to ensure optimal performance in accordance with the datasheet specifications. It is not advisable to exceed these or design to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
$I_{FL}$	Input current, low level	0	250	μA
$I_{FH}$	Input current, high level	6.3	15	mA
$V_{CC}$	Supply voltage, output	4.5	5.5	V
$V_{EL}$	Enable voltage, low level	0	0.8	V
$V_{EH}$	Enable voltage, high level	2.0	$V_{CC}$	V
$T_A$	Operating temperature	-40	+85	°C

## 7. Electrical optical characteristics at Ta=25°C

Parameter		Symbol	Conditions	Min.	Type	Max.	Unit
Input	Forward voltage	$V_F$	$I_F=10\text{mA}$	-	1.33	1.75	V
	Reverse breakdown voltage	$B_{VR}$	$I_R=10\mu\text{A}$	5	20	45	V
	Input capacitance	$C_{IN}$	$V=0, f=1\text{kHz}$	-	70	-	pF
	Temperature coefficient of forward voltage	$\Delta V_F/\Delta T_A$	$I_F=10\text{mA}$	-	-1.4	-	mV/°C
Output	High level supply current	$I_{CCH}$	$V_{CC}=5.5\text{V}, I_F=0\text{mA}, VE=0.5\text{V}$	-	6.5	10	mA
	Low level supply current	$I_{CCL}$	$V_{CC}=5.5\text{V}, I_F=10\text{mA}$	-	9	13	mA
	Low level enable current	$I_{EL}$	$V_{CC}=5.5\text{V}, VE=0.5\text{V}$		-0.8	-1.6	mA
	High level enable current	$I_{EH}$	$V_{CC}=5.5\text{V}, VE=2.0\text{V}$		-0.6	-1.6	mA
	High level enable voltage	$V_{EH}$	$V_{CC}=5.5\text{V}, I_F=10\text{mA}$	2.0			V
	Low level enable voltage	$V_{EL}$	$V_{CC}=5.5\text{V}, I_F=10\text{mA}^{(1)}$			0.8	V
Transfer characteristics	High level output current	$I_{OH}$	$V_{CC}=5.5\text{V}$ $V_O=5.5\text{V}$ $I_F=250\mu\text{A}, VE=2\text{V}$	-	-	100	$\mu\text{A}$
	Low level output voltage	$V_{OL}$	$V_{CC}=5.5\text{V}$ $I_F=5\text{mA}$ $I_{CL}=13\text{mA}, VE=2\text{V}$	-	0.35	0.6	V
	Input threshold current	$I_{FT}$	$V_{CC}=5.5\text{V}$ $V_O=0.6\text{V}$ $I_{OL}=13\text{mA}, VE=2\text{V}$	-	3	5	mA
Isolation voltage	$V_{ISO}$	$R_H<50\%$ $T_A=25^\circ\text{C}$ $I_{I-O}\leq 50\mu\text{A}$	3750			$V_{RMS}$	
Isolation resistance	$R_{I-O}$	$V_{I-O}=500\text{V}$	$10^{12}$			$\Omega$	
Isolation capacitor	$C_{I-O}$	$f=1\text{MHz}$		0.6		pF	

## 7.1 Switching characteristics

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5\text{ V}$ ,  $I_F = 7.5\text{ mA}$  unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Type	Max.	Unit
Propagation delay time to output high level	$T_{PLH}$	$C_L=15\text{pF}$ $R_L=350\Omega$ $T_A=25^{\circ}\text{C}$ (Fig. 12)	20	41	75	ns
Propagation delay time to output low level	$T_{PHL}$		25	50	75	ns
Pulse width distortion	$ T_{PHL}-T_{PLH} $		-	5	35	ns
Output rise time(10%-90%)	$t_r$		-	30	-	ns
Output fall time(90-10%)	$t_f$		-	10	-	ns
Enable propagation delay time to output high level	$t_{ELH}$	$I_F=7.5\text{mA}$ , $V_{EH}=3.5\text{V}$ , $R_L=350\Omega$ , $C_L=15\text{pF}$ (Fig. 13)		15		ns
Enable propagation delay time to output low level	$t_{EHL}$			40		ns
Common mode transient immunity (at output high level)	$ CM_H $	$T_A=25^{\circ}\text{C}, I_F=0\text{mA}$ $ V_{CM} =50\text{V(Peak)}$ $V_{OH}=2.0\text{V}, R_L=350\Omega$ (Fig. 14)	5000	10000	-	V/ $\mu\text{s}$
Common mode transient immunity (at output low level)	$ CM_L $	$I_F=7.5\text{mA}, V_{OL}=0.8\text{V}$ $R_L=350\Omega, T_A=25^{\circ}\text{C}$ (Fig. 14)	5000	10000	-	V/ $\mu\text{s}$

## 8.Characteristic curves

Fig.1 Low Level Voltage vs. Temperature

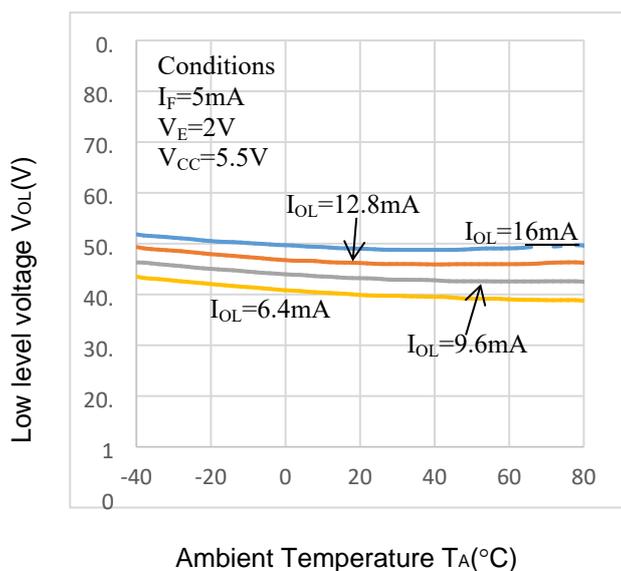
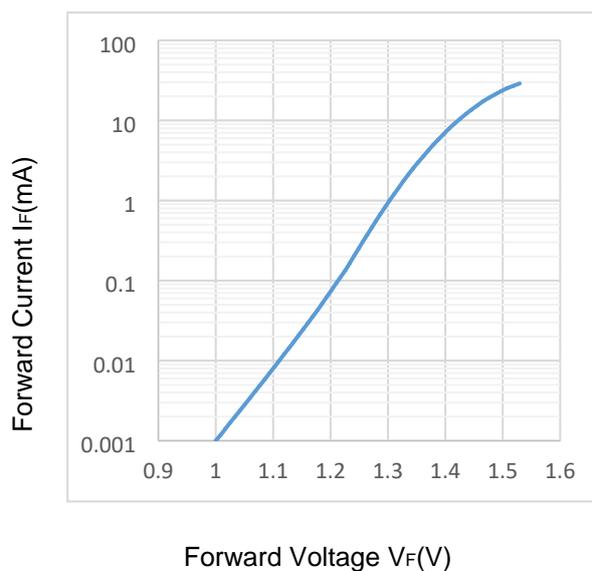
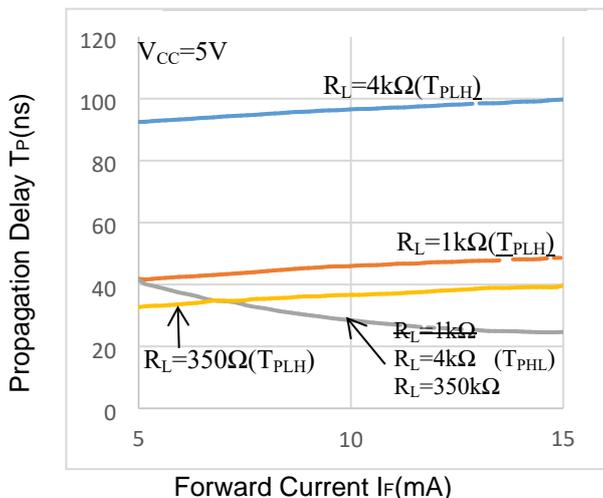


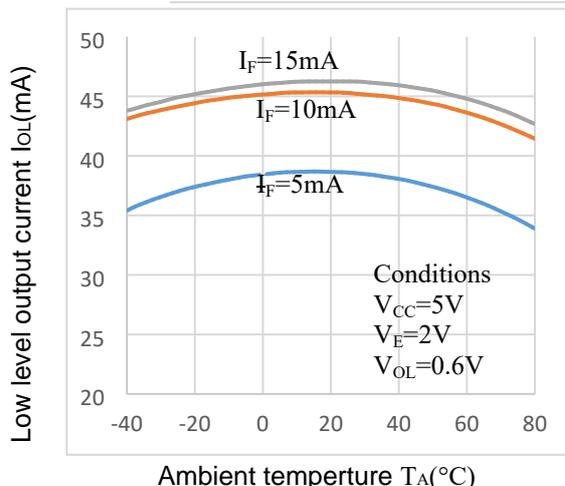
Fig.2 Forward Voltage vs. Forward Current



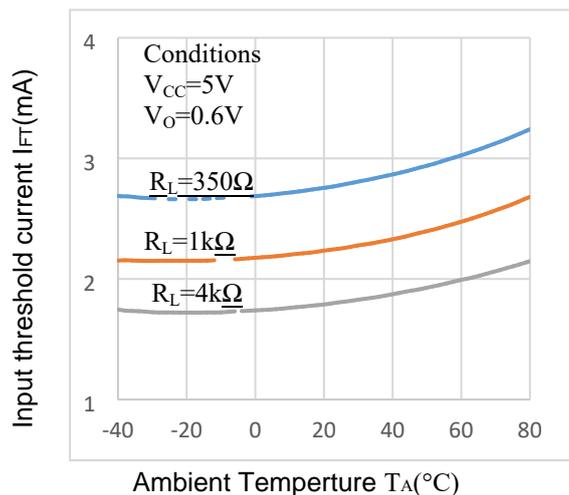
**Fig.3 Switching Time vs. Forward Current**



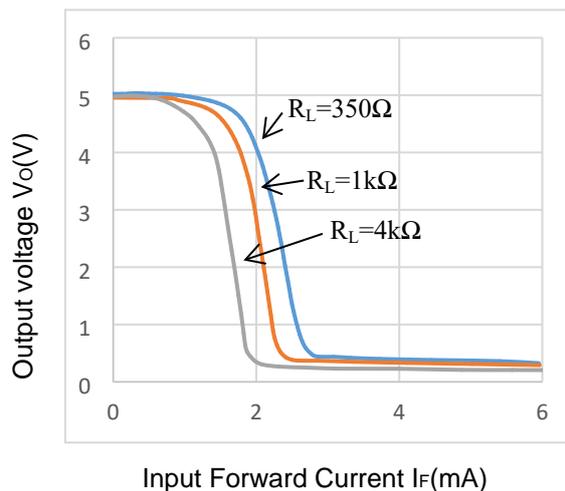
**Fig.4 Low Level Output Current vs. Ambient Temperature**



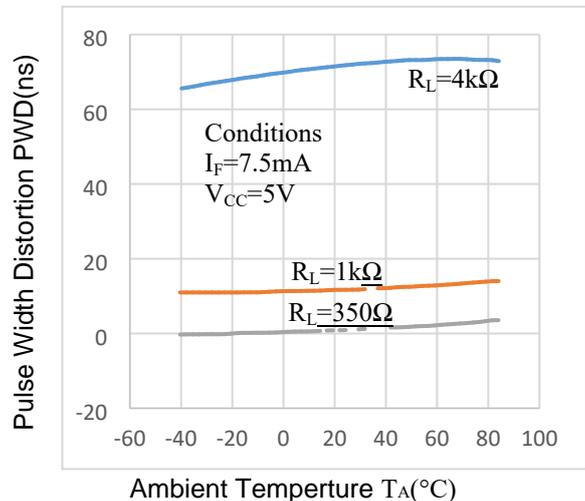
**Fig.5 Starting Current vs. Ambient Temperature**



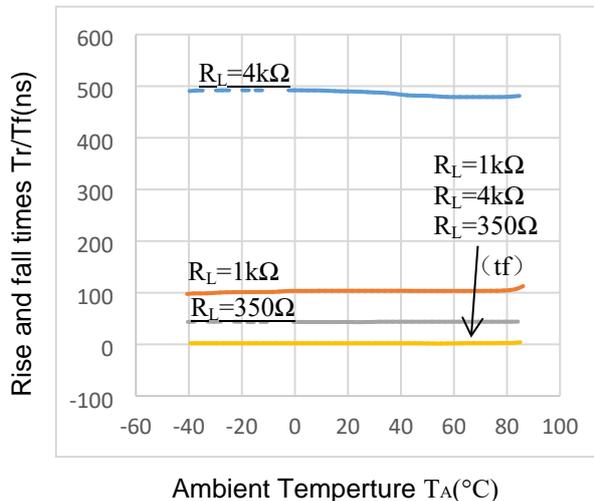
**Fig.6 Output Voltage vs. Input Forward Current**



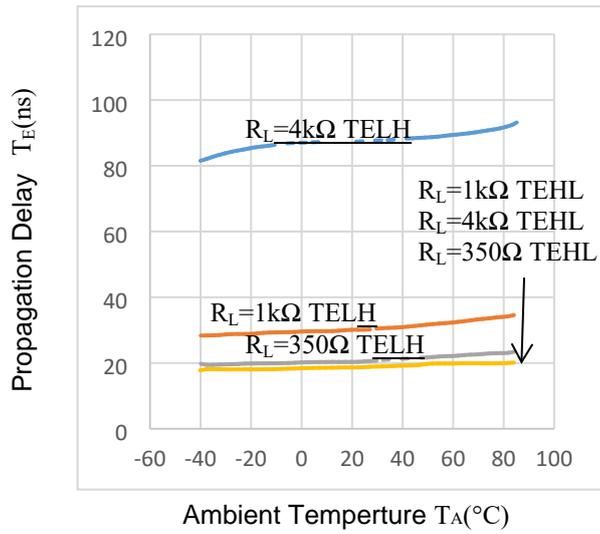
**Fig.7 Pulse Width Distortion vs. Ambient Temperature**



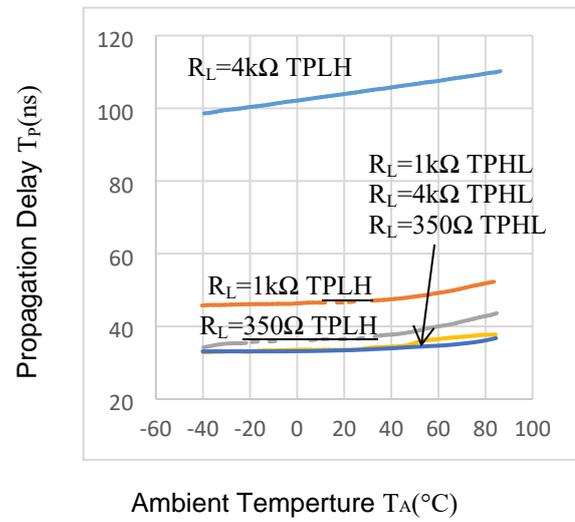
**Fig.8 Rise and Fall Times vs. Ambient Temperature**



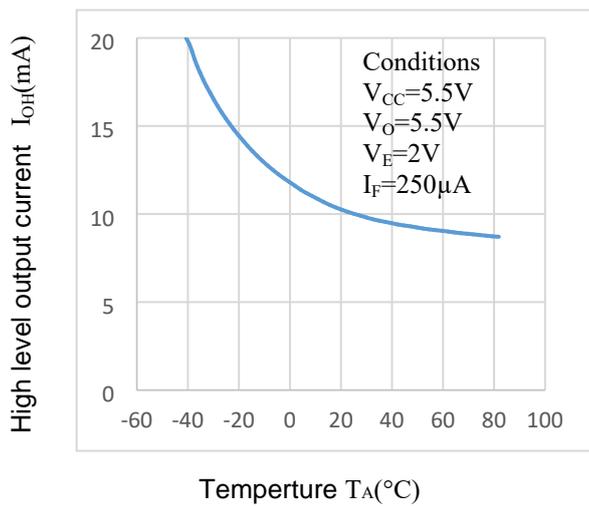
**Fig.9 Enable Propagation Delay vs. Ambient Temperature**



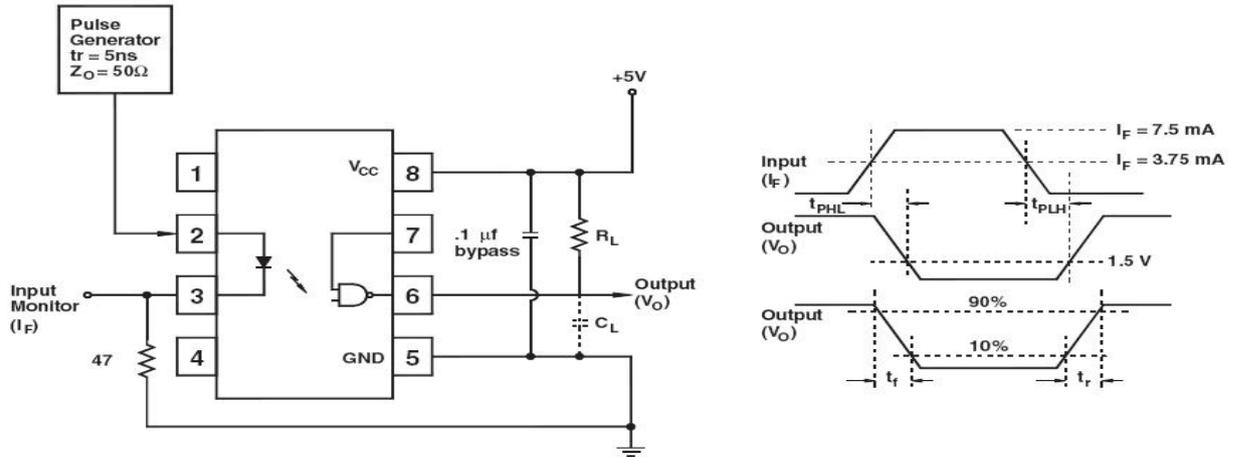
**Fig.10 Switching Time vs. Ambient Temperature**



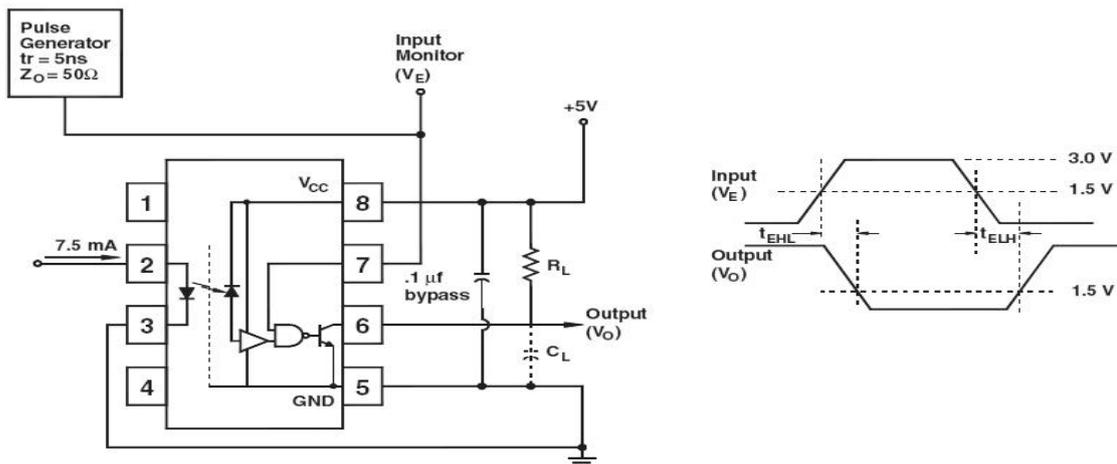
**Fig.11 High Level Output Current vs Temperature**



**9. Test Circuit**



**Fig. 12 Test Circuit and Waveforms for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$  and  $t_f$**



**Fig. 13 Test Circuit  $t_{EHL}$  and  $t_{ELH}$**

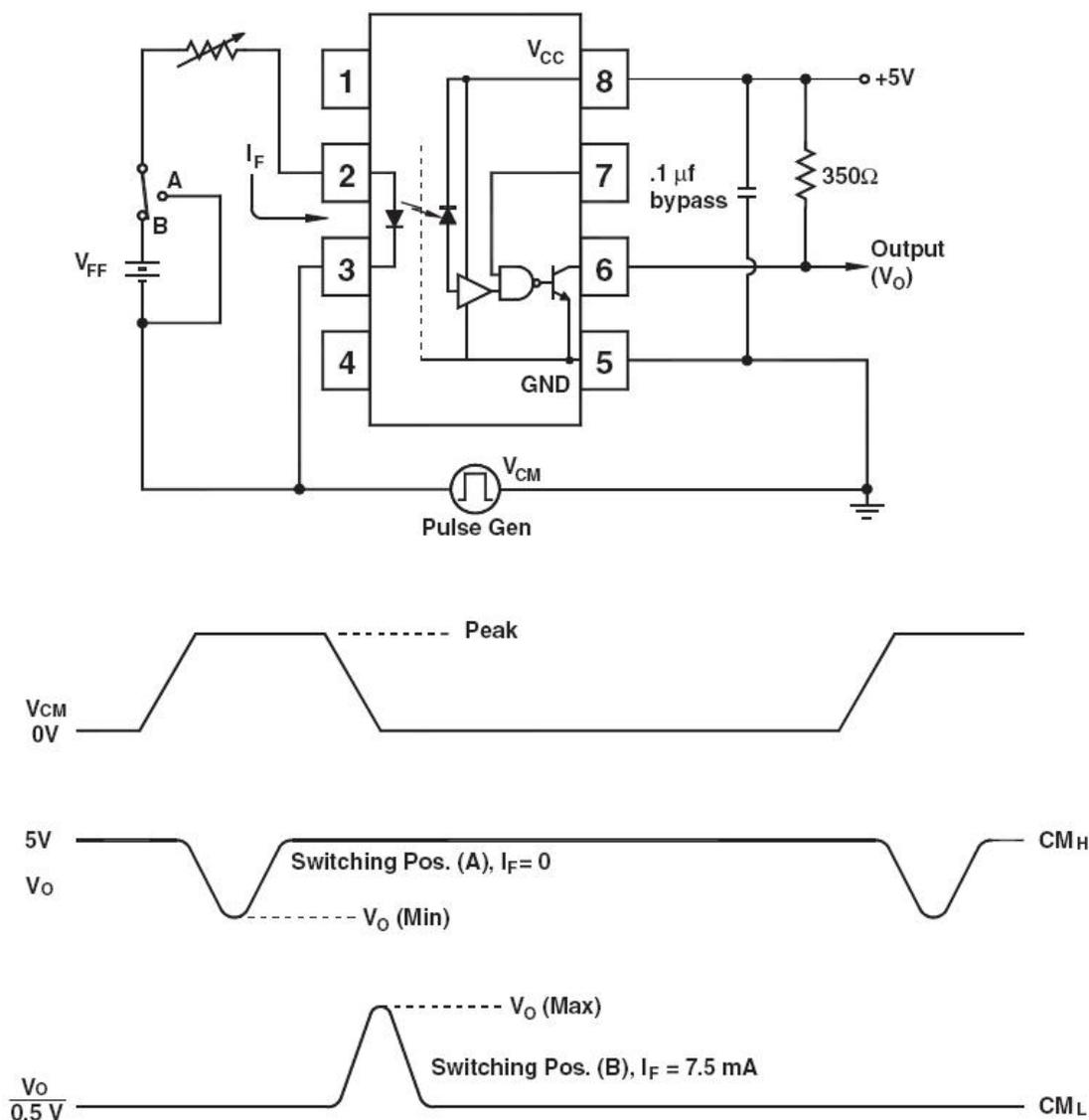


Fig. 14 Test Circuit Common Mode Transient Immunity

**10. Package dimensions**

